Receiver Architecture suitable for Devices in Wireless Body Area Networks

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Outline

• Targets
• System Design
• Results
• Plans
Targets

- 1mW in active mode
- 1uW in standby
- 1mm$^2$ chip area in 65nm CMOS
- 250 kbit/s

- Receiver chain from antenna to decoder
- Medium Access Control (MAC)
- Propagation in bio-applications
System Design
System Parameters

Frequency band: 2.4GHz ISM
+ Wide band, many channels
- Lot of disturbances

Modulation: Wideband FSK
+ Efficient transmitter
+ Low spurious emissions
+ Fits homodyne receiver

Transmit power: -10dBm

Sensitivity: -97dBm (125kbit/s mode)

Can handle up to 87dB path loss (93 dB without SAW)

Modulation

Wideband FSK
+ Efficient transmitter
+ Low spurious emissions

Parameters
* 250kb/s
* $\Delta f = +/- 250$kHz

Spectrum of modulated signal (unfiltered)
PLL loop filter further suppresses sidebands

Observe mid band null => Fits homodyne receiver
Modulation, in IQ-baseband

Wideband FSK
* 250kb/s
* $\Delta f = +/- 250$kHz

One full turn per symbol
Direction depends on databit

How to demodulate?
Demodulation

4 samples/bit used => matched filter for "0" = 1, -j, -1, j
"1" = 1, j, -1, -j

Easily implemented

Magnitude comparison of matched filter outputs => decision
+ No AGC or information about absolute phase needed

Soft information for analog decoder: magnitude difference
Matched Filter Response

Suppression both at DC and channel edges
**Sensitivity**

**Decoder on:**
Thermal noise: -174dBm/Hz  
Noise Figure: 13dB  
Eb/No: 10dB  
Datarate: 125kbit/s  
SAW filter loss: 3dB  
Sensitivity = -174 + 13 + 10 + dB10(125k) + 3 = -97dBm

**Decoder off:**
Thermal noise: -174dBm/Hz  
Noise figure: 13dB  
Eb/No: 12dB  
Datarate: 250kbit/s  
SAW filter loss: 3dB  
Sensitivity = -174 + 13 + 12 + dB10(250k) + 3 = -92dBm
Impact of Imperfections – Time offset

4 samples/bit = 1MS/s = 1us resolution
Max error = 0.5us
Maximum loss = 0.3dB @ BER .001
Bit synch: Selection between 4 time delays sufficient
Impact of Imperfections – 1/f noise

50kHz 1/f noise corner => 0.5dB degradation
Impact of Imperfections – IM2

Spectrum of interfering WiFi signal and the 2nd order intermodulation

With IIP2 = 0dBm, a -37.5dBm WiFi interferer will desensitize by 3dB
Transmitter

Circuit fabricated

- PLL based
- FSK modulation
- Full integration
- Fast settling
- Low power

System simulation of transmitter output
More System Aspects

Can be found in the journal paper:

Results
Antennas and Propagation

2.45 GHz ISM-band for on-body communication investigated, 90dB path loss capability enough for:

- Ear to ear
- Around torso
- Mouth to device
Several front-ends designed in 65nm CMOS

Latest one measures:
- NF<10dB, Gain = 40dB,
- IIP3=-5dBm & IIP2=30dBm @ 10MHz offset
- 0.55mW from 0.85V supply
Analog to Digital Converter

- Continuous-Time (CT) ΔΣ-ADC eliminates analog channel select filter
- 2\textsuperscript{nd} order modulator with 4 bit quantizer
- Single operational amplifier to save power

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured performance</th>
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<tbody>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>800 mV</td>
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<tr>
<td>Active area</td>
<td>0.08mm\textsuperscript{2}</td>
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<tr>
<td>Signal bandwidth</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Maximum input amplitude (-3dBFS)</td>
<td>200 mV differential</td>
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<tr>
<td>Clock frequency</td>
<td>16 MHz</td>
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<tr>
<td>Power consumption</td>
<td>76 \textmu W</td>
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Peak SNDR = 64dB
Baseband

- Combined Decimation and Channel Select Filter
- Sharp filtering in digital domain
- Synchronization
- Demodulation
- Decoding

- Analog and digital decoders measured and compared
- Power consumption of few uW

- 65nm chips with rest of baseband under measurement
We use

- very low power wake-up receiver
- transmitter for data and beacons
- high performance data receiver

all being switched off when not in use.

**50uW -90dBm WUR just measured**

Carl Bryant, Nafiseh Mazloum
Plans

• <3 months remaining of project
  o Transmitter
  o Full receiver chip

• Startup company

• New research projects

Cooperation welcome!